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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/663,755	09/17/2003	Sterling Smith	MSS0007-US	3830

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EXAMINER	
NGUYEN, HIEP	
ART UNIT	**PAPER NUMBER**
2816	

DATE MAILED: 07/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/663,755	SMITH, STERLING	
	Examiner	Art Unit	
	Hiep Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 May 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 3 and 4 are rejected under 35 U.S.C.102 (b) as being anticipated by Peterson et al. (US pat. 5,926,217).

Regarding claim 1, figures 3, 4 and 5c show an interface circuitry of a display chip comprising: an input node receiving an analog input signal from the output of infrared image sensor (111); an adjustable filter (117, col.1, lines 59-61) providing a bandwidth in response to a display mode; a clamping circuit (131) for clamping the processed image signal during a clamping interval.

Regarding claims 3 and 4, the clamping circuit (131) comprises transistor (M9). The connection of the clamp circuit is shown in figure 3

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Olmstead et al. (USP. 5,814,803) in view of Kanagawa et al. (USP. 6,366,866).

Regarding claim 1, figure 10A of olmstead shows an interface circuitry of a display chip comprising: an input node (CCD) for receiving an analog input signal with a display mode; a filter (274); a clamping circuit (S1). Figure 10A of Olmstead does not show that the filter is adjustable. Figure 3 of Kanagawa shows an adjustable filter for adjusting the bandwidth of the analog input signal according to the display mode. Therefore, it would have been obvious to

those skilled in the art to replace the fixed filter of Olmstead with the adjustable taught by Kanagawa for adjusting the bandwidth according to the display mode.

Regarding claim 2, resistor (2111) of the filter (211) is a variable resistor.

Regarding claim 3 and 4, it is well known in the art that clamping switch (S1) is a transistor having a control node controlled by a clamping signal (see US. 6,724,245, Fig.1).

Claims 5 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Peterson et al. (US pat. 5,926,217) in view of Kwon et al. (US Pat. 6,724,245).

Regarding claims 5 and 6, figures 3 and 4 of Peterson include all the limitations of claims 5 and 6 except for the limitation that the clamping circuit comprises a variable resistor and a transistor. Figure 1 of Kwon shows a clamping circuit comprising a variable resistor (N1) and a transistor (N2) for adjusting the voltage at the internal node (col. 5, lines 12-33). Therefore, it would have been obvious to those skilled in the art at the time the invention was made to replace the clamping circuit (131) of Peterson with the clamping circuit taught by Kwon for adjusting the voltage at the internal node. The transistor is transistor (N2) and the clamping signal is (clamp_en). It is inherent that the circuit of Peterson works in display mode.

Claims 7-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Obie et al. (US Pat. 5,038,096) in view of Olmstead et al. (US Pat. 5,814,803), Kwon et al. (US Pat. 6,724,245) and Kanagawa et al. (US Pat. 6,366,866).

Regarding claims 7 and 8, figure 1 of Obie shows an interface circuitry of a display chip comprising;

an input node for receiving an analog image signal with a display mode a to video filter (112);

a video filter (112) for processing said analog image signal and providing a processed image signal at internal node;

an ADC unit (118) for converting said processed image signal into a digital image signal. Figure 1 of Obie does not show a clamping circuit connecting between said internal node and a reference level and the filter is adjustable. Figure 10A Olmstead

shows an interface circuitry of a display chip comprising a clamping circuit (131) connecting between said internal node and a non zero reference level for establishing a precise reference for each pixel before video bump occurs (col. 12, lines 47-57) . Figure 3 of Kanagawa shows an adjustable low-pass filter (211) for eliminating high frequency noise. Therefore, it would have been obvious to those skilled in the art at the time the invention was made to implement the clamping circuit taught by Peterson into the circuit of Obie for establishing a precise reference for each pixel before video bump occurs and to replace the fixed video filter (112) with the adjustable filter (211) taught by Kanagawa for eliminating high frequency noise. The variable resistor is element (2111).

Regarding claims 9 and 10, the combination of Obie, Olmstaed and Kanagawa includes all the limitations of claims 9 and 10 except for the limitation that the filter comprises a variable resistor and a capacitor. Figure 1 of Kwon shows a clamping circuit comprising a variable resistor (N1) and a clamping transistor (N2) controlled by signal (clamp_en) for adjusting the voltage at the internal node (col. 5, lines 12-33). Therefore, it would have been obvious to those skilled in the art at the time the invention was made to replace the clamping circuit (S1) of Olmstead with the clamping circuit taught by Kwon for adjusting the voltage at the internal node. The clamping transistor is transistor (N2) and the clamping signal is (clamp_en).

Regarding claims 11 and 12, the variable resistor is element (N1) of Kwon and the transistor is (N2) receiving a control signal (clamp_en).

Response to Arguments

In the Remarks, page 7, the Applicant argues that the predetermined bias voltage Vdet is not an analog image signal. In figure 3 of Peterson, element (111) is an thermal infrared image sensor and the voltage change across the thermal infrared sensor is small (col. 4, lines 10-31). Vdet is a bias voltage for activating the infrared sensor. The circuit of figure 3 is the unit cell corresponding to a pixel of a focal plane array (fig. 1 or 2). The output of the unit cell is sent to a video system to be processed (col. 3, lines 4-23). Figure 5c shows the unit cell output that is an analog video signal. Thus, the voltage change across the infrared sensor (111)

is an analog image signal. Note that, it is well known in the art that the infrared sensor is an image sensor (see USP. 6,851,894 and 4,302,774).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hiep Nguyen whose telephone number is (571) 272-1752. The examiner can normally be reached on Monday to Friday from 7:30am to 4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on (571) 272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Hiep Nguyen

12-07-05

TUAN T. LAM
PRIMARY EXAMINER